Tunable Optical Delays, Buffering and WDM:TDM Conversion via Active Latin-Routing AWG's featuring Unit-Length Re-Circulating Waveguides

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Abstract: Stepped and scaleable 64-increment optical buffering and time-delay provision via two concatenated 8×8 arrayed-waveguide gratings is described, requiring only 1.6% of typical total waveguide-length. A method to reduce computational effort and to minimize waveguide crossovers during device design is also discussed. Finally, we demonstrate perfect dispersion for WDM:TDM conversion for 16 wavelengths/time-slots.

Keywords: Optical delays, optical buffering, arrayed-waveguide gratings, optical packet switching, WDM, TDM

1. Introduction

Optical packet switching is emerging as an important technology for supporting next-generation IP-over-optics networks. In addition, optical-based signal processing, access network edge switching, and optical-interconnects within computing systems are becoming key technologies for future high bit-rate data transmission and manipulation. In the context of optical buffering and memory, e.g. fine synchronisation in optical TDM systems, multiplexing/de-multiplexing at the edge of the switch fabric, or timeslot interchange, a selectable optical-delay device is of great importance for efficient operation. There have been various suggestions for optical delay-lines based on photonic crystals [1], ring resonators [2,3], electromagnetically-induced transparency [4], coupled cavity optical waveguides [5] etc. However, each of these technologies offers a compromise between complexity, tunability, available bandwidth, speed and size.

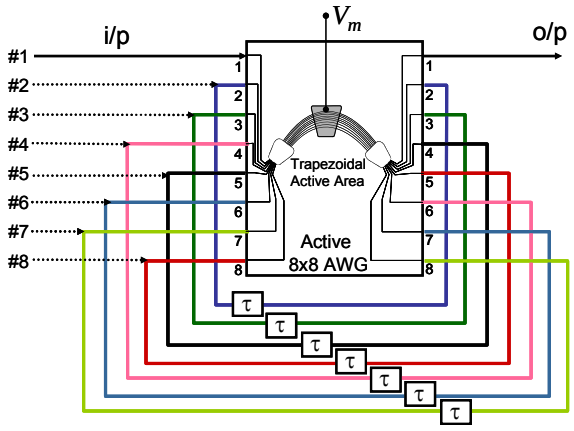

Figure 1: Stepped 8-increment time-delay and selectable memory flexibility for re-circulating, uniform waveguide-length, Latin-routing active AWG.

In this paper, we present a reconfigurable optical delay architecture based upon a tunable arrayed-waveguide grating (AWG) within a concentric uniform-length re-circulating configuration. Previous proposals using AWGs for selectable time delays have simply used a set of waveguides of increasing length used only once for each selected time delay [6]. Such a scheme does not scale well with increasing number N of selectable time delays, since the overall summed length of waveguide track increases as $N(N\text{-}1)/2$, increasing polynomially with N, and so is expensive in terms of chip real estate. However, we can take advantage of the Latin routing [7] characteristic of an AWG to achieve a tunable optical-delay device whose overall waveguide track length simply increases linearly with N. Additionally, by employing an active AWG with an active trapezoidal region [8] at its centre (Fourier plane) acting as a tunable prism, we can dynamically select optical delays in a reconfigurable manner. Appropriate re-circulating configurations connecting AWG o/p ports back to the i/p ports for an $N\times N$ AWG were initially found using an exhaustive search in C, which was then refined to reduce the search space.

2. Latin-Routing Recirculating Configuration

Fig.1 shows the schematic layout for an 8×8 device solution, which illustrates the non-redundant re-circulating geometry of our delay-line design. We note that the inherent bidirectional nature of the AWG and the overall architecture allows reflection at the output port to double the allowable delay. For a signal entering at input port #1, the time-delay associated with each m^{th} AWG internal Latin-routing configuration is shown in the first row of Table 1. Although the time-delays do not increase monotonically with m, the full range of possible delays between 0 and 7τ is possible. The entry and exit ports at the input and output planes as shown in Fig.1 represent a canonical disposition. Scrolling variation of the entry and exit port dispositions whilst keeping them laterally symmetrical yields the same functionality. However, skewed disposition of the input and output ports simply yields a cyclic permutation of the columns of Table 1. Here, the additional memory functionality of our design is indicated, when the extra design flexibility of varying entry port # at the input plane of the AWG is exploited (shown by dotted lines in Fig.1). Signals can enter at any of the ports 2-8 via a coupler or appropriate optical circulator, so that the basic re-circulating functionality of the device is preserved. Table 1 illustrates one of the interesting properties of our re-circulating design, as certain configurations of control voltage V_m and i/p port have no defined exit; this being a labyrinthine confinement. This has possible applications for medium-term optical memory, since the signal will recirculate through the maze

with a time-delay (indicated by the number in italics in Table 1) for each loop.

input port #	V_0	V_1	V_2	V_3	V_4	V_5	V_6	V_7
1	**0**	**5**	**6**	**7**	**2**	**1**	**3**	**4**
2	*1*	**4**	**3**	**4**	*5*	*5*	*4*	**0**
3	*1*	**3**	**5**	**2**	*5*	*5*	**0**	**1**
4	*5*	**1**	*1*	**1**	*5*	**0**	*4*	**2**
5	*5*	**2**	**2**	**6**	**0**	*5*	**1**	*1*
6	*5*	*1*	**1**	**0**	*5*	*5*	**2**	*2*
7	*5*	*1*	**0**	**5**	*5*	*5*	*4*	**3**
8	*5*	**0**	**4**	**3**	**1**	*1*	*4*	*2*

***Bold**: Selectable time delay;*
Italic: Selectable memory buffer size.

Table 1: Selectable optical time-delays/buffer size with input port # of 8×8 AWG and single exit port #1.

Data can be read from the particular memory store by changing the AWG internal Latin-routing state. Assuming one packet per loop-back waveguide, the number in italics in Table 1 also indicates the number of packets which can be stored in memory for that particular configuration. We note that the number of bits per time delay is a design choice, and can be scaled up. Multiple data streams (up to N-1 in number) can be stored in such a configuration, e.g. Table 1 shows that 5×5 packets and 2×1 packet lengths (i.e. 7 streams consisting of 27 packets in total) can be stored within the device for the m=0 configuration. Table 1 also indicates the result of using the AWG in its wavelength-division multiplexing (WDM) role where multiplexed wavelengths are introduced at the input port #1. In this case, the AWG passively routes the wavelengths to the appropriate output ports, according to its Latin routing and WDM-demultiplexing capability, with each wavelength seeing a different Latin-routing configuration, and is either buffered or delayed by the indicated amounts. Varying the control voltage V_m changes the delay times or memory configurations accordingly. In the case of concatenated N×N AWG's, the first device consists of re-circulating unit-delay tracks (c.f. Fig.1), whereas the second device comprises N×unit delay tracks. The output port #1 of the first AWG feeds directly into the input port #1 of the second device. Using two 8×8 active AWG's this allows any integer time-delay between 0 and 63τ to be selected, using only a total of (7×1)+(7×8)=63 unit length waveguides, in a compact geometry. This is in contrast to a total waveguide length of 4032 units for the non-recirculating design [6], thus our design represents a 98.4% reduction in waveguide length requirements.

3. Design Method

Software was written in C to determine how the AWG and delay-lines should be interconnected in order to realise every integral delay between 0 and $N-1$, where the AWG setting determines the delay. Each possible connection pattern between the outputs of the AWG and its inputs may be represented by a permutation on the set {1, 2, …, N – 1}. For each of the (N – 1)! permutations, the software examines all N possible configurations of the AWG, and if every delay from 0 to N – 1 is generated as a result, a valid solution is recorded. Although efficient algorithms exist to enumerate all permutations [9], the overall solution is extremely time-consuming to implement, having execution time of $O(N^{N+1})$, hence only results for $N \leq 14$ could be generated with the time and computing resources available. It is desirable for the control voltage on the AWG to be directly proportional to the delay, however, only one such solution has been found, for N = 4. No solutions were found for odd values of N, but for even N, the total number of solutions is shown in Table 2.

N	2	4	6	8	10	12	14
solutions	1	2	0	64	416	5960	142380

Table 2: Number of solutions for different sizes of AWG

4. Minimum Cross-Over Topologies

To enhance execution speed, the set of permutations under consideration was restricted by reducing the number of waveguide crossovers, also facilitating implementation. In the mathematical theory of permutations, assuming some permutation π, the notation $(a\ b\ c\ \ldots\ z)$ means that $\pi(a) = b$, $\pi(b) = c$, and so on, up to $\pi(z) = a$. This concept is helpful when simplifying the search algorithm, where all connections in a cycle are close together on the range u to v where $v - u + 1 \geq c$, and each cycle is of the following generic type:

$$(a_1\ a_2\ \ldots\ a_{i-1}\ a_i\ a_{i+1}\ \ldots\ a_n\ b_1\ b_2\ \ldots\ b_{j-1}\ b_j\ b_{j+1}\ \ldots\ b_m)$$

where $n + m = c$, $a_i < a_{i+1}$, $b_i > b_{i+1}$, $a_1 = u$, $b_1 = v$, and each connection is represented in the cycle exactly once. It can be shown that such cycles imply exactly $c - 1$ waveguide crossovers when realised. This may be called a "bitonic cycle", after the definition by Batcher of a bitonic sequence [10]. Here are some examples of bitonic cycles on six elements:

(1 3 5 6 4 2)
(1 5 4 3 2 1)
(1 3 4 6 5 2)

Further reductions in complexity may be realised, for example, by restricting the sizes of cycles and their order, thus reducing the search space further. While these concepts have been used to generate solutions for N up to 32, no simple general solution has been found. Analytical proofs show that for $N \geq 8$, the solutions are organised into groups of four through symmetry. However, no other patterns are evident in the results, and work continues on finding solutions for large N.

5. "Perfect Dispersion" Solutions

Certain external connection configurations connecting the AWG output plane to the input plane yield a "perfectly dispersive" optical true-time delay situation. This occurs when the time delays associated with the set of cyclic (internal routing) Latin routing permutations increase monotonically as the set of Latin routing possibilities is cycled. Such a perfectly dispersive device can be used for WDM to TDM conversion, or alternatively find applications in phased-array antennas. For example, the 4×4 devices of Fig.2 have external connections designed to exhibit

perfect dispersion. If a WDM multiplexed signal is input into the device, the wavelengths emerge each delayed by a time in proportion to its wavelength. In Fig.2, considering the first AWG only, the dotted, dot-dashed, solid and dashed lines represent the internal Latin mapping routes of four (increasing) wavelengths λ_1,λ_2,λ_3 and λ_4, representing one free-spectral range (FSR) of the device, which are delayed by 0, τ, 2τ and 3τ respectively. In addition, where the AWG's FSR is designed such that it is equal to $N\times\Delta\lambda$ (where $\Delta\lambda$ is the wavelength spacing between adjacent WDM channels), sending a signal consisting of multiple WDM channels spanning more than one FSR causes the WDM channels to be demultiplexed into one of N time slots, according to the relative position of each WDM channel in the FSR.

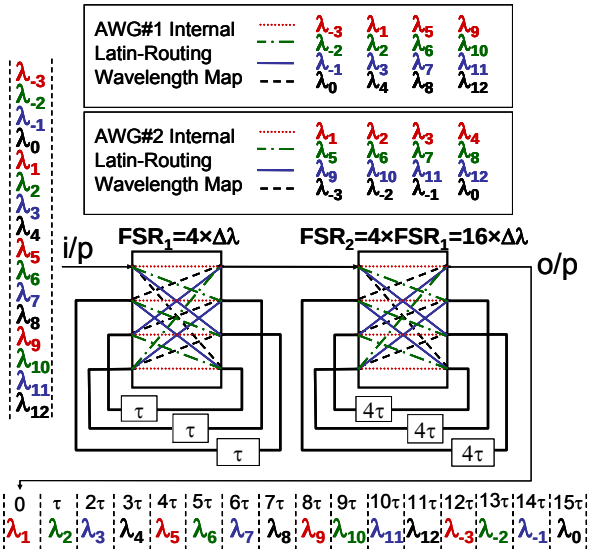

Figure 2: TDM:WDM sorter using two concatenated true-time delay passive 4x4 AWG's.

Fig.2 additionally shows concatenation of two cascaded 4×4 perfect-dispersion devices to allow 16 different time delays. To achieve appropriate delays for all the wavelengths, the second device's FSR and passband channel width are each increased by a factor N; with the waveguide lengths (and hence delays) in the second device also increased by a factor of N. Thus the two cascaded 4x4 devices are functionally equivalent to a single 16x16 device. We note that in this case the AWG's are all passive in nature (i.e. the internal mappings are not actively changed) and rely on the natural dispersive (demultiplexing) nature of an AWG. Fig.2 indicates 16 wavelength channels spanning four FSR's of the first AWG and occupying the same time slot, being temporally demultiplexed into 16 consecutive timeslots, monotonic according to the wavelength.

6. Conclusions

We have described a novel scaleable and reconfigurable optical-delay and buffering device, based on a Latin-routing AWG, which exhibits a full-complement of selectable optical delays in a compact, flexible and integrated design. Such a device may find important application in WDM:TDM optical switching architectures, router buffers and emerging true-time delay phased array antenna applications.

7. References

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