

CHIST-ERA Projects Seminar Day 2, Cross Topics Heterogeneous Distributed Computing

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Heterogeneity and Distribution In Action

This presentation was written by these people:





Oh, no! No More Moore Anymore

Dennard Scaling



Power C area



Dennard Scaling

1974-2005

Power 🛠 area



Oh, no! No More Moore Anymore

Moore's Law



Transistor count doubles every 2 years



Law

1965-2015

TSMC: Per transistor cost rises in 2015!

shutterstock

HAPPY NEW YEAR



Fat CPU





Fat CPU



Small CPUs





Fat CPU





GPU

Small CPUs





Fat CPU





GPU

Small CPUs



FPGA



But doesn't fit on one machine



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- Too hard to program
 - CPUs, GPUs, FPGAs complex interactions
 - Massive distribution complex network
 - Must optimise at multiple scales
 - Only experts can play

Chist-era Chist-era

- Too much energy
 - ~20MW each, 1.5% globally, growth exponential







- Machines internally heterogeneous
- Machines heterogeneous to each other
- Massive distributed networks
- Networks heterogeneous
- Very hard to program
- If we don't get it right => energy/performance disaster



The Projects

HPDCJ

Heterogenous Parallel Distributed Computing in Java

DIONASYS

Declarative and Interoperable Overlay Networks, Applications to Systems of Systems

DIVIDEND

Distributed Heterogeneous Vertically IntegrateD Energy Efficient Data centres



The Projects

	HPDCJ	DIVIDEND	DIONASYS
Programming Model	✓	✓	✓
Dependability	✓		
Data Management	✓	✓	✓
Versatility		✓	✓
Optimisation Techniques		✓	
Distributed Techniques	✓	✓	✓

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High Performance Computing

Parallel distributed computing in Java

PCJ library for parallel computing in Java

- Scalability up to 6000 cores
- CPU and GPGPU
- Fault Tolerance

- Easy for non expert programmers
 - New approach to teach students

DIONASYS

System as a first-class component (holon)

- Generative programming
- Application in IoT

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System Composition

Self organising overlays Prototypes Open Sourced





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DIVIDEND

- Vertical integration
- Programming model
- Energy accounting
- Auto tuning
- More heterogeneity
- Fast networks

Prototypes Open Sourced Already saving 22% energy



Chistera Grand Challenge

Write a program, then system automatically

- Chooses the right hardware
 - Or creates new hardware
- Optimises everything
- It is easy for the programmer

Roadmap

In 5 Years we need

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- Programming models for major domains
- DSLs to specialise to all devices (CPU, GPGPU, FPGA)
- Eliminate waste in computing
- SDN needs to be transparent the application



Roadmap

In 10 Years we need

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- Universal languages for the masses
- Tool chains to co-design platforms and fabricate logic/network/memory blocks for services
- Programming without knowing what's out there





Provide new calls

- Parallel programming
- Energy optimisation
- Automatic hardware synthesis

Conclusion

Energy/performance crisis looming

• Can't program and optimise HDC

• We are making progress on this

Need more calls on this

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