

Plasticity in NEUral rmristive Architectures

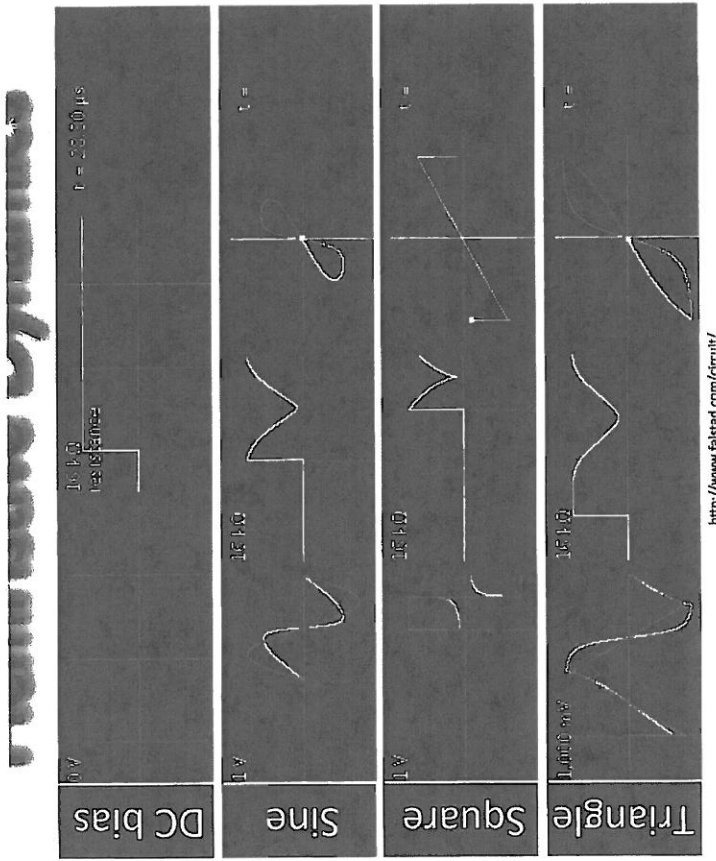
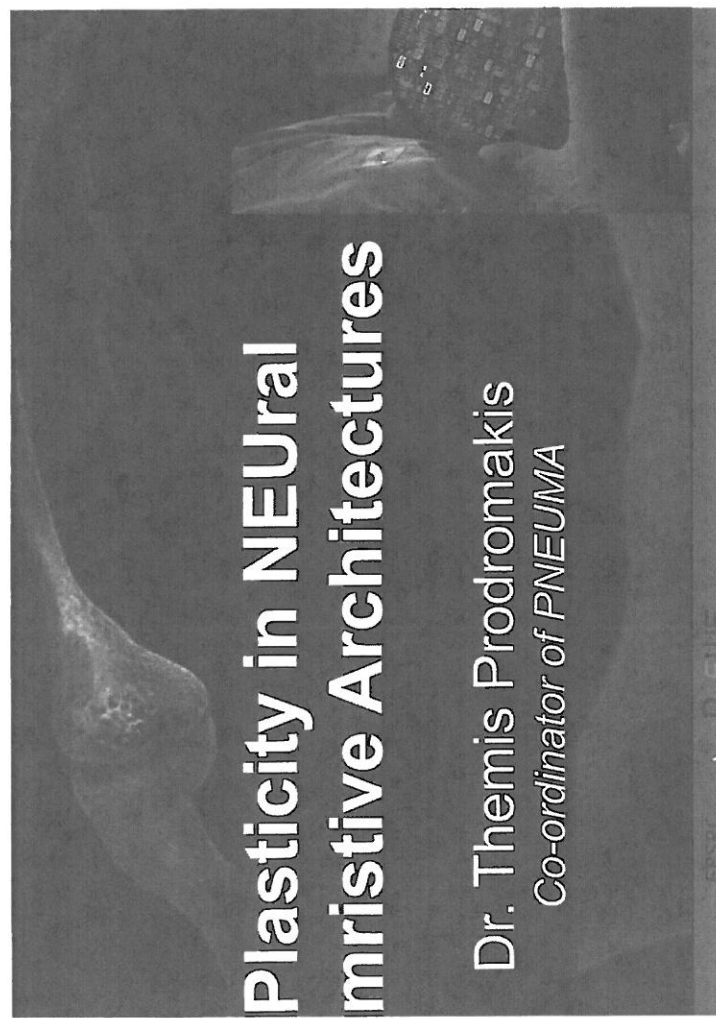
Dr. Themis Prodromakis
Co-ordinator of PNEUMA

Intentionally planted deficiencies are introduced in a very controlled way, allowing them to be displaced under appropriate biasing.

Memristor-the missing circuit element," IEEE Trans. Circuit Theory, vol. 18, 1971.

The charge displacement alters the overall conductance of the device.

R. Williams, "How we found the missing memristor," IEEE spectrum, vol. 45, 20



Memristive dynamics can be exploited in many practical applications, with particular emphasis in the areas of analogue IC design and neurobiology

Analogue and digital circuits are revisited...

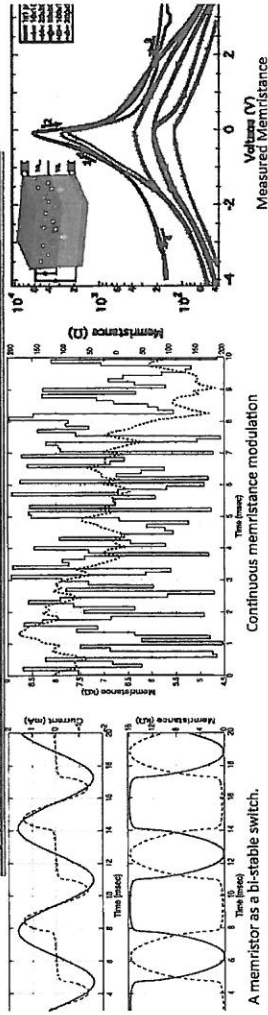
- memory
- logic
- dynamic loads
- chaotic oscillators
- synapse emulator
- adaptive systems
- associative memory
- retinomorphic processing

...while novel bio-mimetic designs are facilitated.

Memory

Traditional and Emerging Memory Technologies

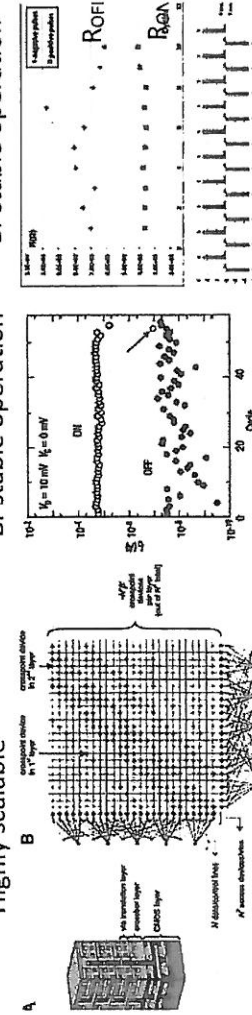
Knowledge level	Traditional Technologies				Emerging Technologies			
	DRAM	SRAM	Improved Flash	NAND	FeRAM	MRAM	PCRAM	Advanced
Cell Elements	6T	6T	1T	1T	1T1C	1T1R	1T1R	1T1R
Read time (ns)	50	10	10	10	180	130	65	10
Write time (ns)	50	10	10	10	22	45	16	10
Retention time (years)	< 1	< 1	< 1	< 1	< 10	< 10	< 10	< 10
Write/erase time (ns)	< 1	< 1	< 1	< 1	< 10	< 10	< 10	< 10
Read op. voltage (V)	2.5	1.2	1.5	1.5	> 10	> 10	> 10	> 10
Write op. voltage (V)	1.5	1.2	1.5	1.5	0.9-3.3	1.5	1.5	1.5
Write endurance	10 ¹⁵	10 ¹⁵	10 ¹⁵	10 ¹⁵	10 ¹⁴	10 ¹⁴	10 ¹⁴	10 ¹⁴
Write energy (fJ/bit)	6	0.7	1.0	1.0	30	1.5 × 10 ³	8 × 10 ³	8 × 10 ³
Density (Gbit/cm ²)	6.67	0.17	1.23	2.47	0.14	0.13	1.48	1.48
Major technological barriers	Highly scalable	Highly scalable	Highly scalable	Highly scalable	poor	poor	poor	poor



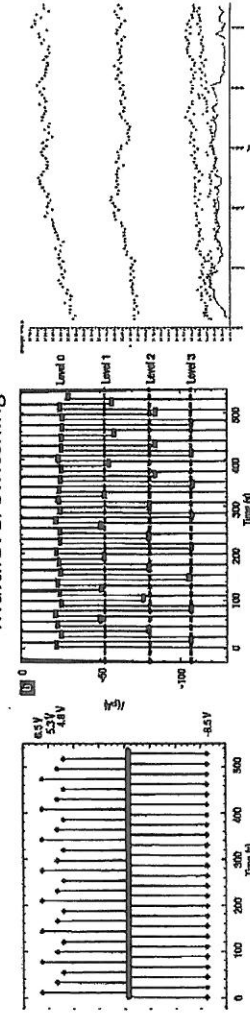
et al., "Switching mechanisms in microscale memristors", IET Elec.Lett., vol. 46, 2010.

Memory

Highly scalable



Multilevel switching

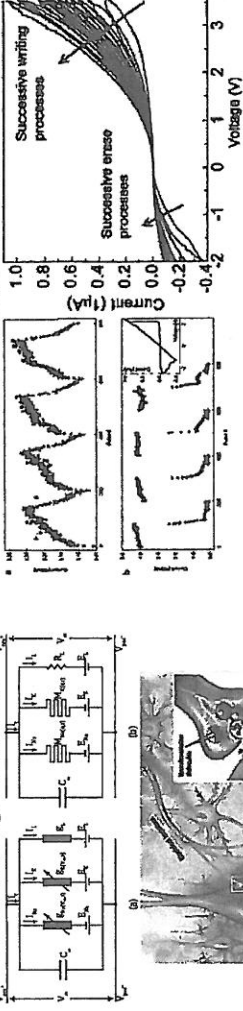


2D-dimensional address topology for circuits with stacked multilayer crossbar arrays", PNAS, vol. 106, no. 48, pp. 20155, 2009.

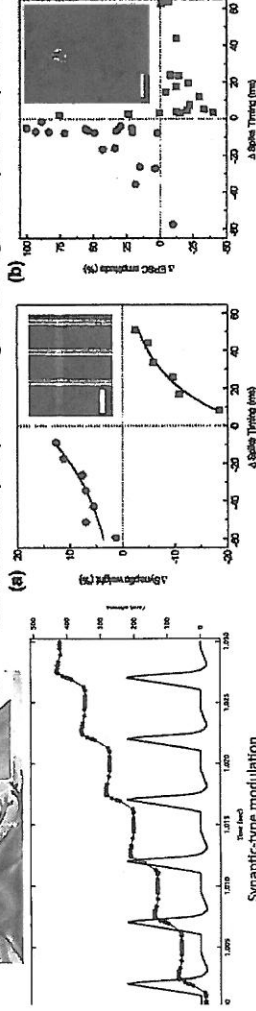
Ionically-based resistive switching memories", Nat. Materials, vol. 6, no. 11, pp. 833-840, 2007.

Synapse emulator

Potentiation/Depression pulses



Measured synaptic weight change vs spike separation



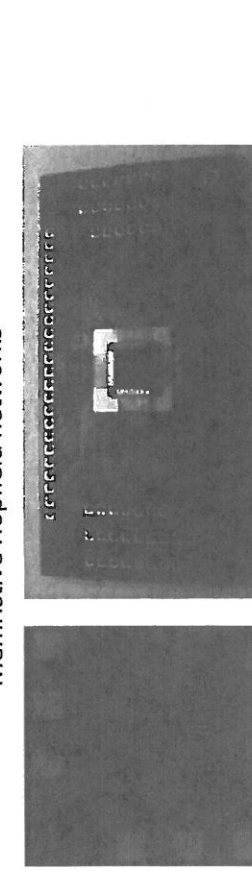
s et al., "A Review on Memristive Devices and Applications", ICECS, Dec. 2010.

Nanoscale Memristor Device as Synapse in Neuromorphic Systems", Nano Lett., vol. 10, no. 4, pp. 1297-1301, 2010.

An electrically modifiable synapse array of resistive switching memory", Nanotechnology, vol. 20, 2009.

Adaptive Systems

Memristive Hopfield networks



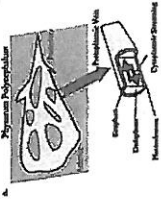
Evaluating the direction of the change of the states of the memristor array:

$$(a^T * (1 - b) + (a^T - 1) * (b))/2$$

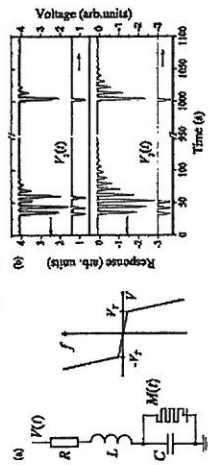
k, B. Jakli and T. Prodromakis, "Cellular neural networks with memristive cell devices", ICECS, Dec. 2010.

Associative memory

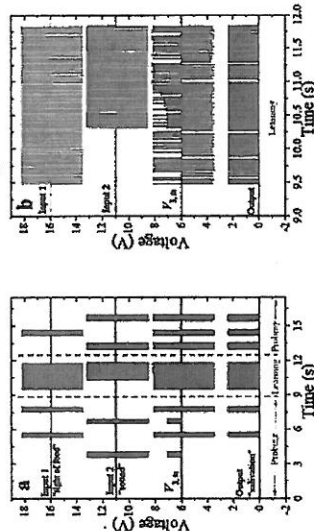
Amoeba's learning



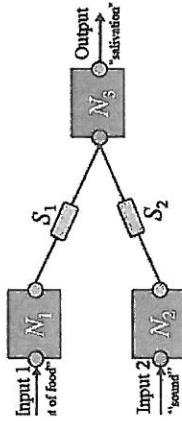
Damping modulation of LC contour



Association of sound and sight of food

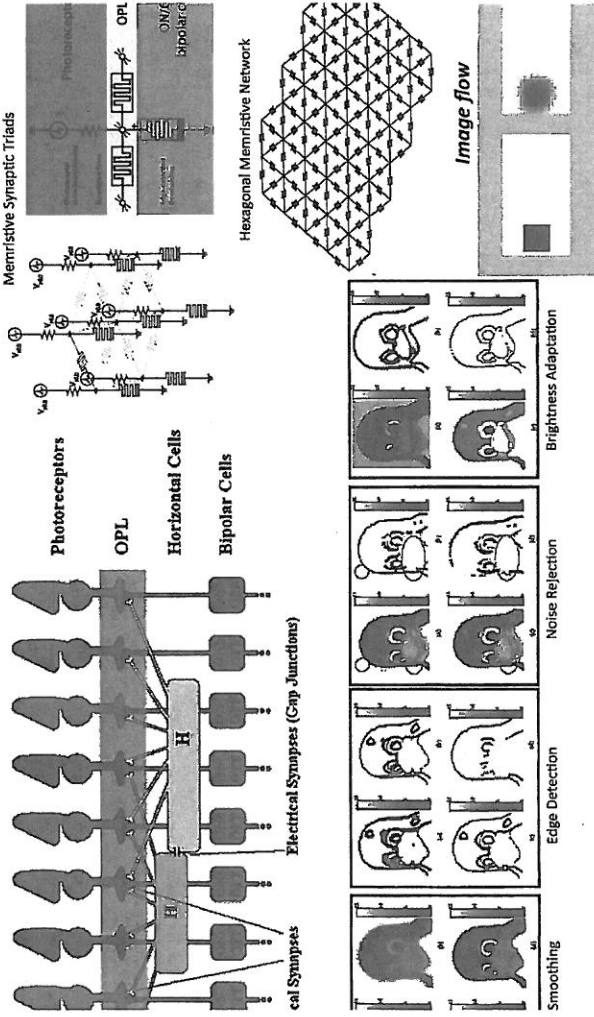


Pavlov's experiment



M. Di Ventra, "Experimental demonstration of associative memory with memristive neural networks", arXiv:0905.2835v3, 2010.
 "Memristive model of amoeba learning", Phys. Rev. E, vol. 80, 2009

Modelling the Outer Plexiform Layer of the retina with Memristive grids



makis et al., "Biomimetic model of the outer plexiform layer by incorporating memristive devices", Phys. Rev. E, 2012.

ST-ERA 1st Call – Beyond Autonomic Systems – the Challenge of Consciousness

Research approach

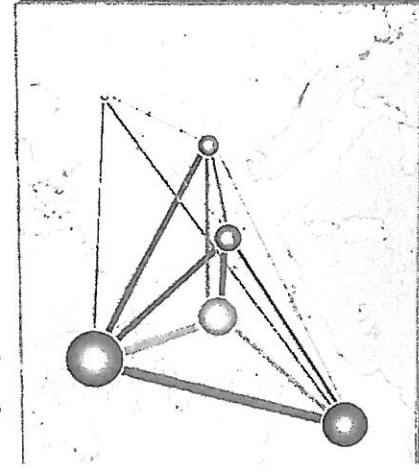
Psychologists, cognitive scientists, clinicians and neuroscientists have strived to provide authoritative definitions of consciousness within a neurobiological framework.

We have more recently joined this quest by developing neuromorphic VLSI circuits for emulating biological functions in artificial systems to recreate attributes such as true processing locality and complexity (10^{10} synapses per cm^2).

We aspire to develop experimental platforms capable of perceiving, learning and adapting to stimuli by leveraging test developments of five leading European institutions in neuroscience, nanotechnology, modelling and circuit design. The non-linear dynamics as well as the plasticity of the newly discovered memristor are shown to support Spike-based Timing-Dependent-Plasticity (STDP), making this extremely compact device an excellent candidate for realizing adaptive self-adaptive circuits; a step towards "autonomous cognitive systems". The intrinsic properties of real neurons as well as their organization in forming neural circuits will be exploited for optimizing CMOS-based neurons, grids and the integration of the two into real time biophysically realistic neuromorphic systems. Finally, the system would be tested with conventional as well as abstract methods to evaluate the technology and its autonomous

chis

Geographical Distribution



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 Der Wissenschaftsfonds
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Institutions

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 London
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Institute of
 neuroinformatics
 University of
 Zurich



LAAS-CNRS
 INSTITUT
 CARNOT
 LAAS
 Université
 de Toulouse

Group Leaders

Prof. Chris Toumazou

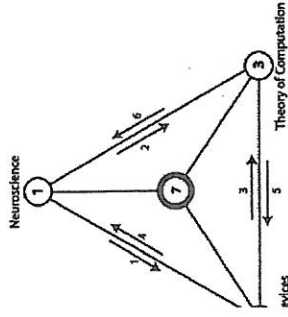
Prof. Bernabe Linares

Dr. Giacomo Indiveri

Dr. Robert Legenstein

Prof. Robert Plana

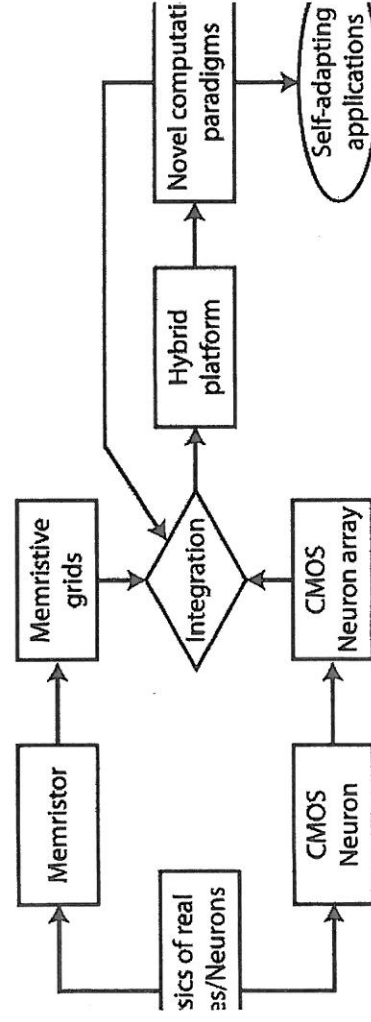
Research interactions



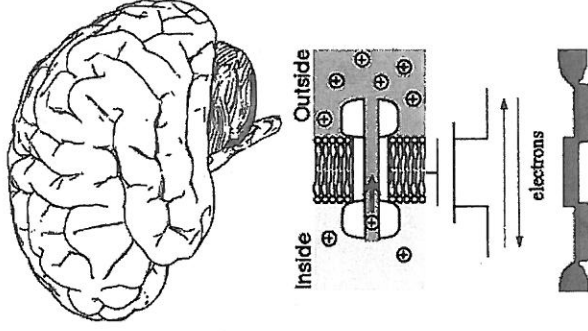
1. Development of biophysically mimetic synapses and neurons
2. Modelling and implementation of neural circuits
3. Development and establishment of novel brain-inspired computational principles
4. Optimisation of device and computational models
5. Practical system-level application of novel computational algorithms
6. Set-up of real-time experiments and benchmarks
7. Development of system-level hybrid CMOS/Memristor platform demonstrate autonomous behaviour

Specific research objectives

Development of robust memristive devices for evaluating existing analytical models. Development of appropriate instrumentation techniques for evaluating (read) and altering (write) distinct states. Study of biophysical mechanisms involved in plasticity and learning that can be mapped to standard analog VLSI and memristor device physics. Design of hybrid memristor/CMOS circuits that operate using the same biophysics of synaptic plasticity in neurons. Development of spike-based computation paradigms. Application of nano-fabrication techniques for resolving integration issues for enhancing the interconnectivity and complexity.



An attractive alternative computing technology

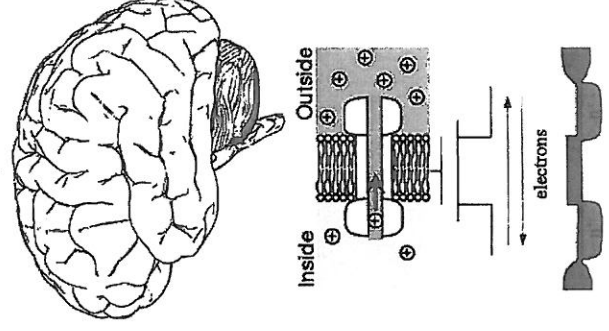


To emulate the principles of computation of neural systems, using standard VLSI (Very Large Scale Integration) technology.

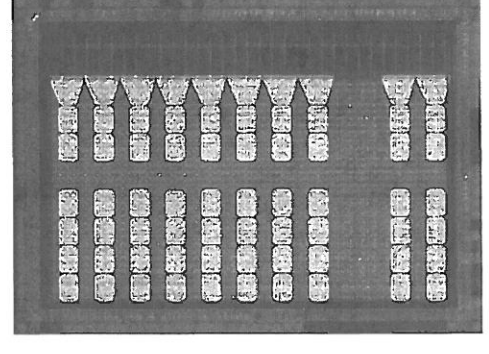
Goals:

- To exploit the physics of silicon to reproduce the bio-physics of neural systems, using analog VLSI circuits.
- To develop multi-chip spike-based computing systems, using asynchronous digital VLSI technology.
- To automatically configure and "program" neuromorphic processing systems to carry out real-time behavioral tasks.

An attractive alternative computing technology



To emulate the principles of computation of neural systems, using standard VLSI (Very Large Scale Integration) technology.



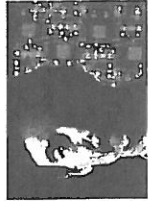
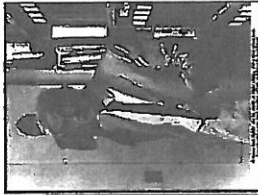
- Analog/Digital
- Asynchronous
- Event-based
- Real-time
- Low-power
- Fault-tolerant
- Compact

The origins

The field of Neuromorphic Engineering has its roots in neuroscience.

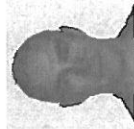
Tom Caltech

- Biology/ Bio-physics (Max Delbrück)
- Physics (Richard Feynman, John Hopfield)
- Engineering (Carver Mead)

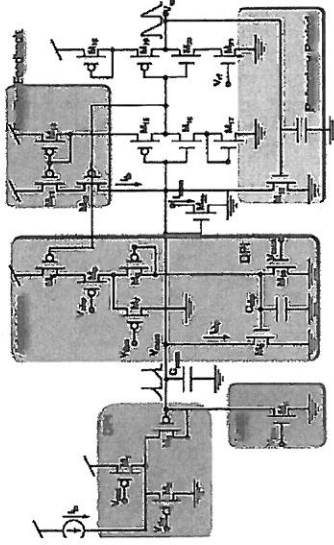


to Oxford and Zurich

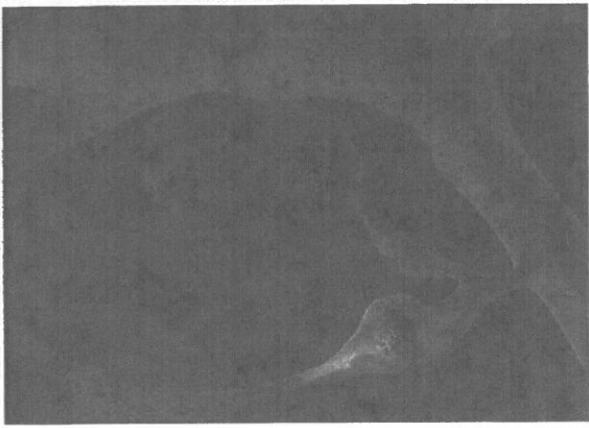
- Engineering and Biology (Carver Mead and Misha Mahowald)
- Neuromorphic engineering and neuroscience (Misha Mahowald, Rodney Douglas, Kevin Martin)



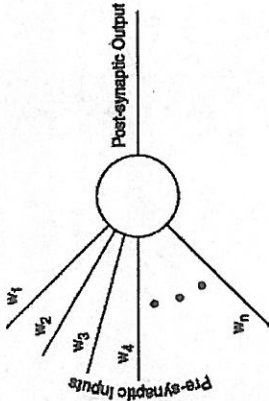
Silicon neurons



Real synapses

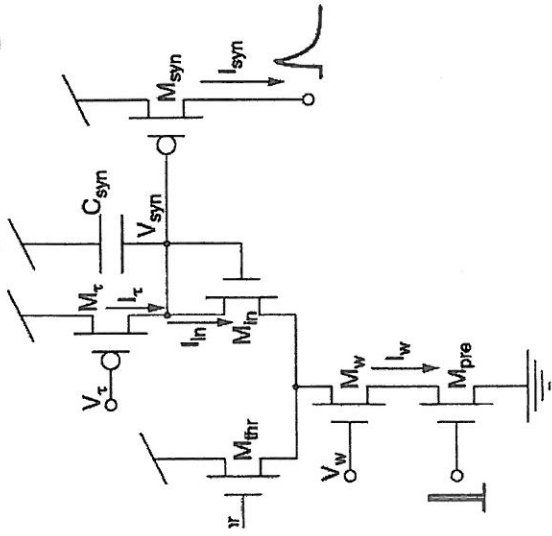


Artificial synapses



Synapses are often modeled as instantaneous multipliers.

Science and Engineering Visualization Challenge
2005 winner, Graham Johnson, *Medical Media*, Boulder,



$$I_{syn}(t) = I_0 e^{-\frac{t}{\tau}} (V_{syn}(t) - V_{dd})$$

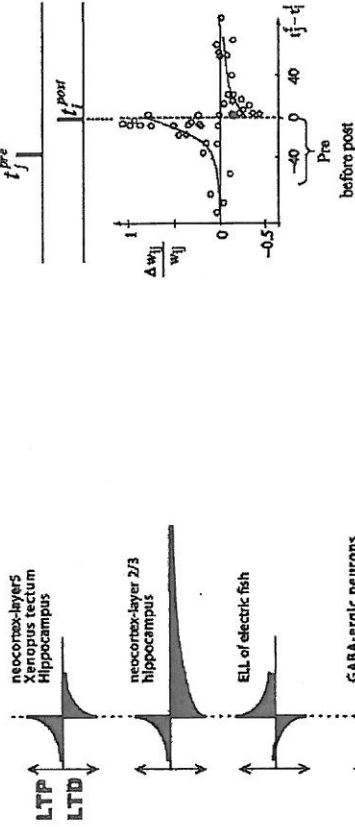
$$I_{thr} = I_0 e^{-\frac{\kappa(V_{thr} - V_{dd})}{U_T}}$$

$$C_{syn} \frac{d}{dt} V_{syn} = -(I_{in} - I_c)$$

$$\tau \frac{d}{dt} I_{syn} + I_{syn} = \frac{I_{thr} I_w}{I_c}$$

[Bartolozzi and Indiveri, *Neural Computation*, 2007]

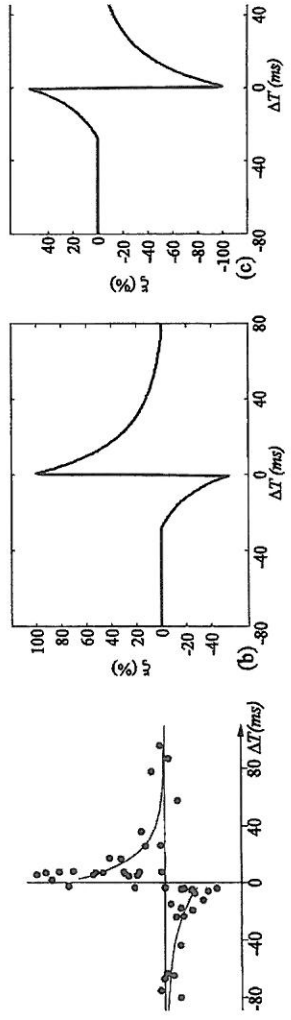
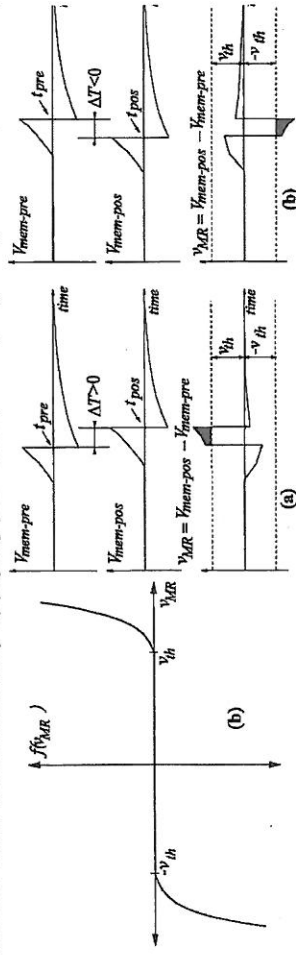
Spike-Timing Dependent Plasticity (STDP)



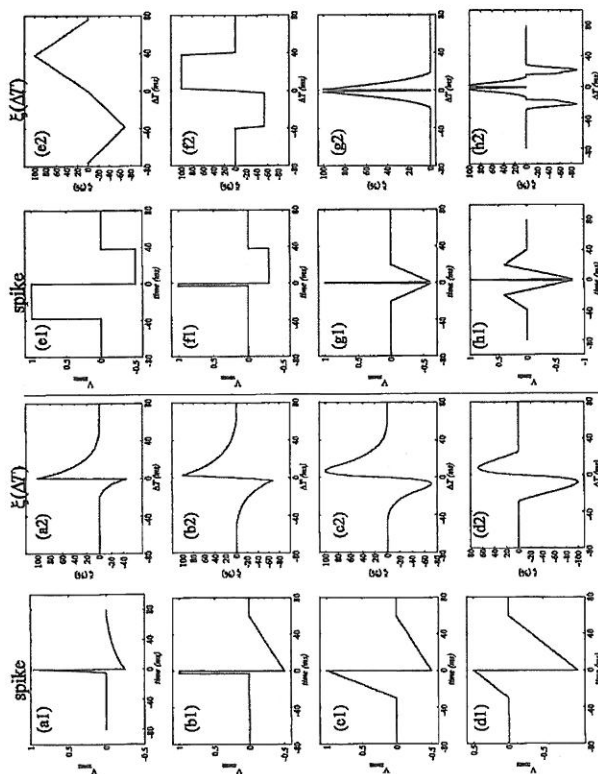
- 1 If a pre-synaptic spike arrives shortly before a post-synaptic spike is emitted, the synaptic efficacy is increased.
- 2 If it arrives soon after the spike is emitted, the synaptic efficacy is decreased.

Abbott, Nelson, 2000

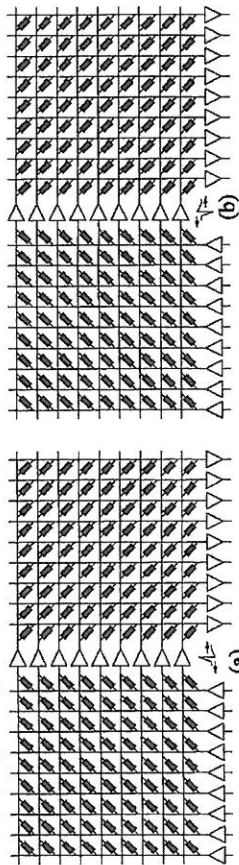
can do STDP with memristors by applying pre- and post-synaptic spikes of specific shal



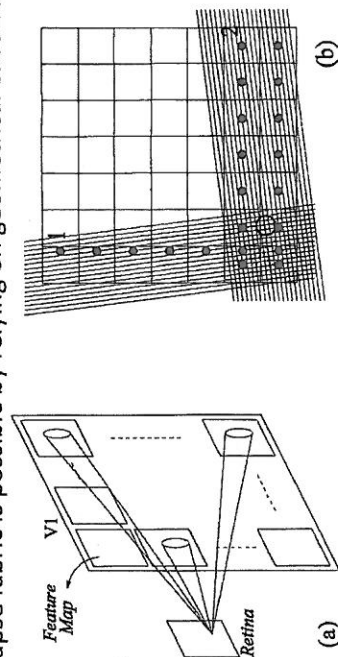
Changing shape of spikes changes STDP learning



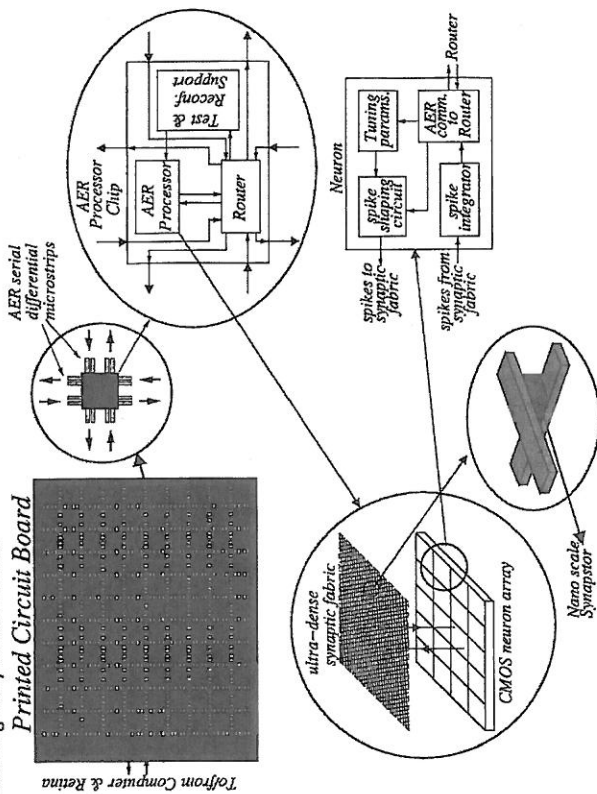
Build hardware by using neurons that send spikes forward and backward asynchronously



Every dense synapse fabric is possible by relying on geometrical CMOL structures



Realistic outlook exploiting STDP-learning neuron chips (each with 10^6 neurons and 10^{12} synapses-memristors) using multi-chip routing and communication to assemble several hundred chips per PC Intercommunicating many of such PCBs.



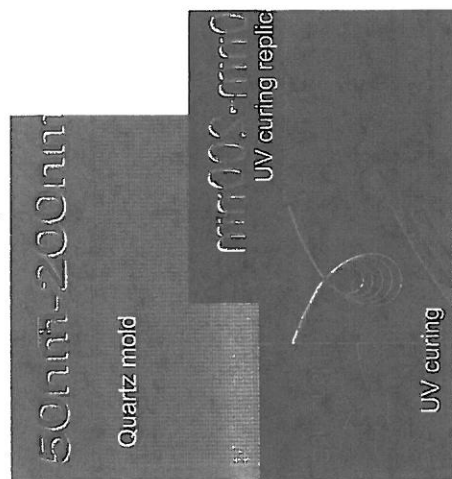
p-chip bonding

The first step towards CMOS integration of processing constrains for memristor device fabrications



Nano-imprint Lithography

- Second CMOS integration step
- quick micro and nanostructures replication
- uses standard photolithography machines (Low cost)
 - UV 400nm
 - alignment
 - resolution limited by the mask



Processing systems

What I cannot create, I do not understand

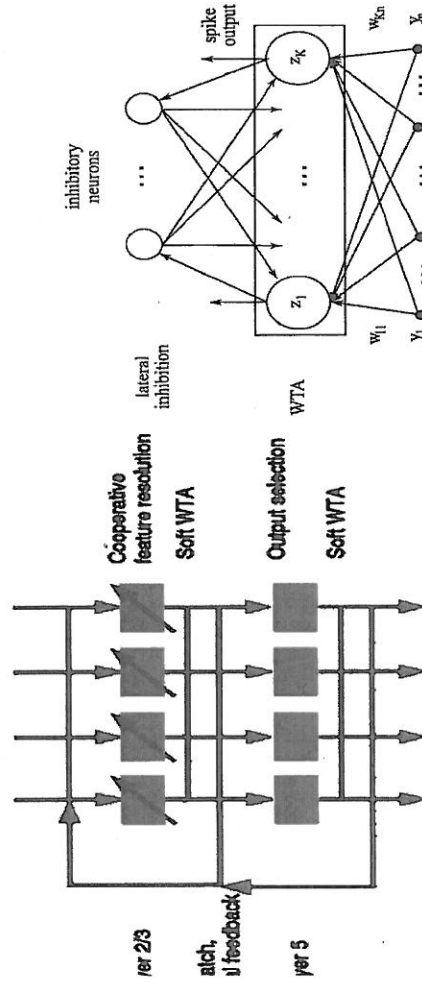
Richard P. Feynman - On his blackboard in his office at Caltech, 1988

building hardware emulations of neural systems, using the same physics of computation with both VLSI and memristive circuits, imposes constraints on the models that are likely to be similar to the ones faced by real neural systems:

- Structure vs. function
- Energy, power consumption
- Area, density, connectivity
- Limited resolution
- Bounded variables
- Inhomogeneities and variability

A canonical microcircuit motif: Winner-Take-All (WTA) circuits

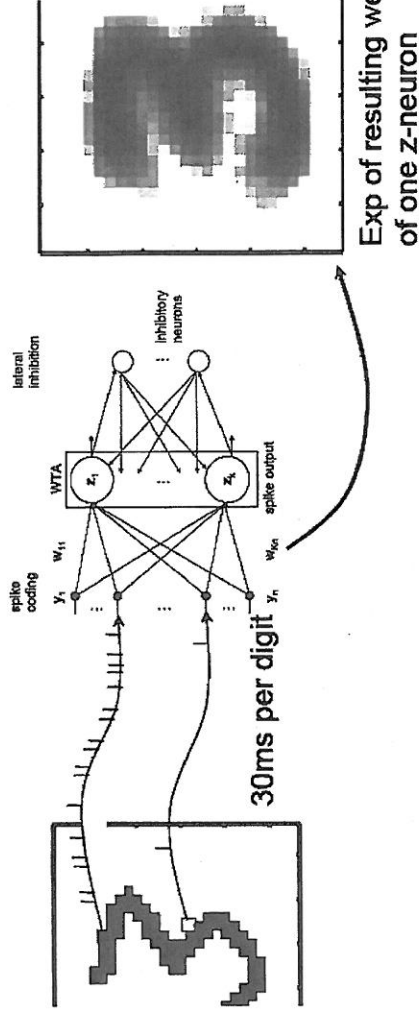
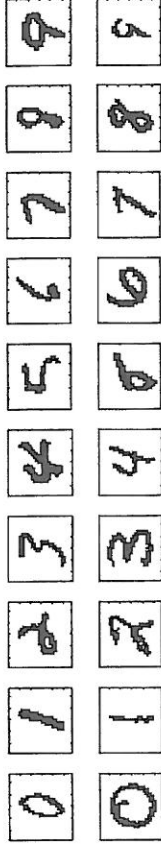
Subcortical, intra-, and inter-areal input



Simple model for a soft WTA circuit

[Douglas and Martin, 2004]:
„canonical microcircuit“ of the cortex

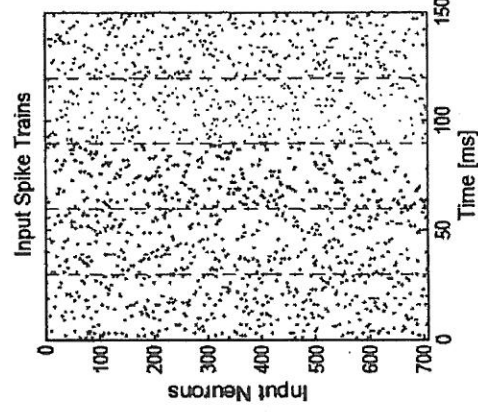
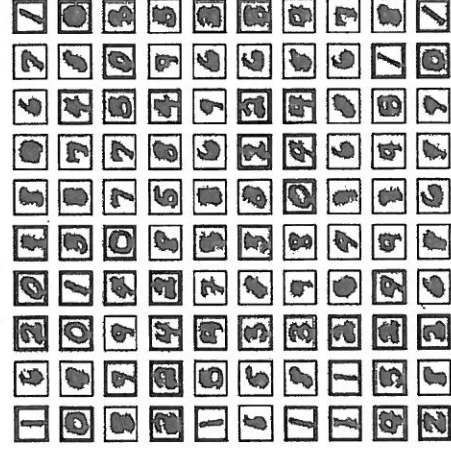
These are 20 random samples from the 70 000 samples in the MNIST dataset.

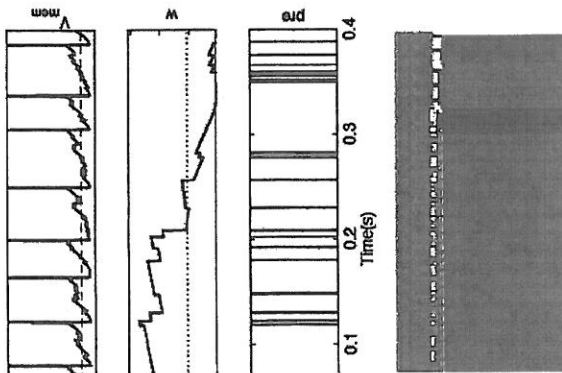


Exp of resulting weights of one z-neuron

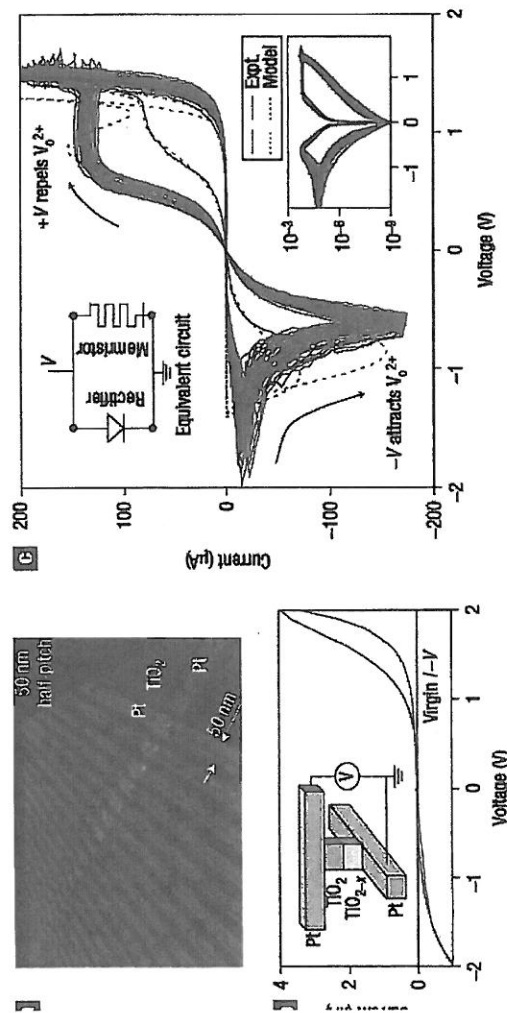
exposing the circuit to 300s of spike inputs (where a different sample of a handwritten digit is encoded in each window of 30 ms) WTA neurons specialize to specific digits.

Synaptic weights of WTA neurons arranged in the 2D input space:



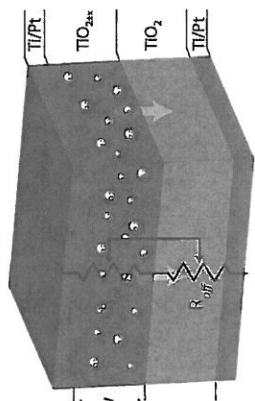


HP's memristor



Bipolar reversible and nonvolatile switching of nanoscale TiO_{2-x} devices

4 a.l., "Memristive switching mechanism for metal/oxide/metal nanodevices", Nature Nanotech., vol. 3, 2008



Memristor cross-section.

$$M(t) = \frac{w(t)}{D} R_{on} + \left(1 - \frac{w(t)}{D}\right) R_{off}$$

$$v(t) = w_0 + \frac{\mu R_{on} q(t)}{D}$$

$$M(q) = R_0 - \frac{\mu R_{on} \Delta R q(t)}{D^2}$$

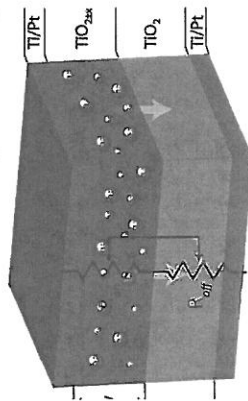
$$R_0 = R_{on} \frac{w_0}{D} + R_{off} \left(1 - \frac{w_0}{D}\right)$$

"The elusive memristor: properties of basic electrical circuits", Eur. Journal of Physics, vol. 30, 2009.

1., "The Missing Memristor Found", Nature, vol. 453, pp. 83-86, May 2008.

SPICE Model of Memristor With Non-linear Dopant Drift", Radioengineering, vol. 18, pp. 210-214, Jun 2009.

et al., "A Versatile Memristor Model With Non-linear Dopant Kinetics", IEEE TED, vol. 58, 2011.



Memristor cross-section.

$$M(t) = \frac{w(t)}{D} R_{on} + \left(1 - \frac{w(t)}{D}\right) R_{off}$$

$$v(t) = w_0 + \frac{\mu R_{on} q(t)}{D}$$

$$M(q) = R_0 - \frac{\mu R_{on} \Delta R q(t)}{D^2}$$

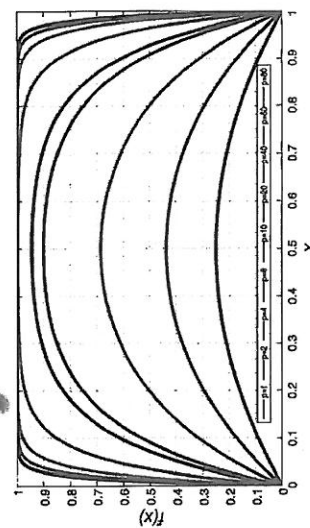
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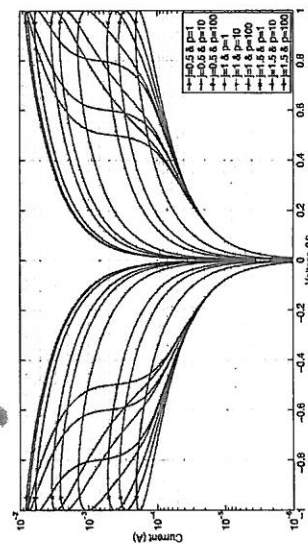


Plot of our proposed window function $f(x) = 1 - [(x - 0.5) / 0.75]^p$ vs p as a variable.

Non-linear dopant drift can be introduced through a window-function $f(x)$.

$$\frac{dx}{dt} = \frac{\mu R_{on} i(t)}{D^2} f(x) \quad \text{with} \quad x = w / D$$

$$f(x) = 1 - \left[\frac{(x - 0.5)^2 + 0.75}{0.75} \right]^p$$

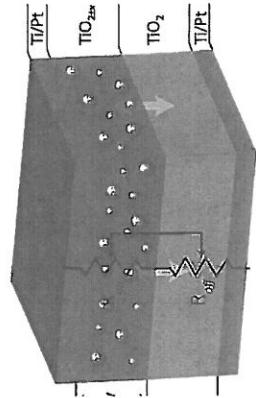


A family of $\log(I)$ - V curves for J and p varying.

Non-linear dopant drift can be introduced through a window-function $f(x)$.

$$\frac{dx}{dt} = \frac{\mu R_{on} i(t)}{D^2} f(x) \quad \text{with} \quad x = w / D$$

$$f(x) = 1 - \left[\frac{(x - 0.5)^2 + 0.75}{0.75} \right]^p$$



Memristor cross-section.

$$V(t) = \frac{w(t)}{D} R_{on} + \left(1 - \frac{w(t)}{D}\right) R_{off}$$

$$w(t) = w_0 + \frac{\mu R_{on} q(t)}{D}$$

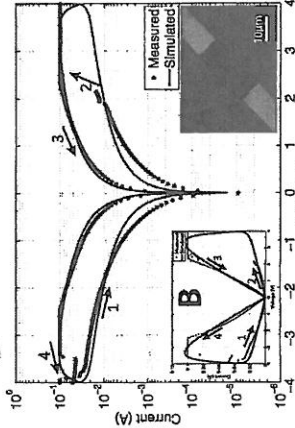
$$V(q) = R_0 - \frac{\mu R_{on} \Delta R q(t)}{D^2}$$

$$R_0 = R_{on} \frac{w_0}{D} + R_{off} \left(1 - \frac{w_0}{D}\right)$$

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$$\frac{dx}{dt} = \frac{\mu R_{on} i(t)}{D^2} f(x) \quad \text{with} \quad x = w/D$$

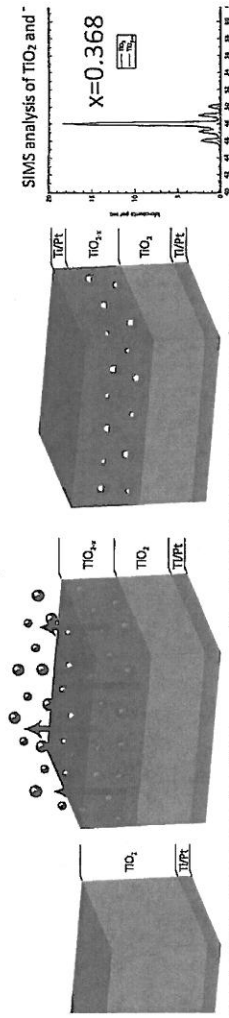
$$f(x) = j \left(1 - \left[(x - 0.5)^2 + 0.75 \right]^p \right)$$



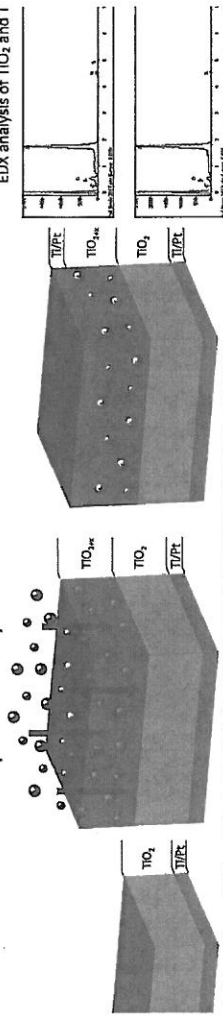
Simulated and measured I-V response of a TiO₂/TiO_{2-x} memristor.

Ways to fabricate memristors

Hewlett Packard's way



Imperial's way



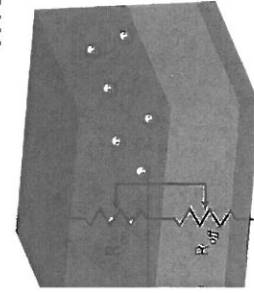
al. "Memristive switching mechanism for metal/oxide/metal nanodevices", Nature Nanotech., vol. 3, 2008
 al. "Electrical and defect thermodynamic properties of nanocrystalline titanium dioxide", J. Appl. Phys., vol. 85, 1999.
 kis, "Electrically actuated switch", GB 1000182.3.
 kis et al., "Switching mechanisms in microscale memristors", IET Elec. Lett., vol. 46, 2010.
 kis et al., "Fabrication and Electrical Characteristics of Memristors with TiO₂/TiO_{2-x} active layers", IEEE ISCAS, May 2010.

Common methods for processing memristors

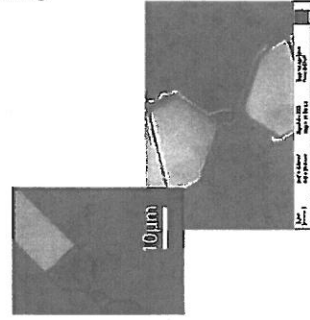
Method	Core Steps	Advantages	Disadvantages	Status
graphy & lift-off	2	Simplicity	Device size, device density	Implemented
e-evap. & lift-off	2	Nano-scale electrode dimensions	Alignment, device density	
y & lift-off, single-step core	1	High-quality core	Device size, complexity, electrical isolation	
am litho & lift-off	2	Nano-scale electrodes, device density	Not suitable for mass-production	Under developme
o-Imprint rography (NIL)	2	Nano-scale electrodes, device density, mass production	-	Under developme
single step	1	High-quality core	Device density	Characterisation
used Ion am (FIB)	1	High-quality core	Not suitable for mass production, contamination	

nakis et al., "Practical micro/nano fabrication implementations of memristive devices", CNNA 2010.

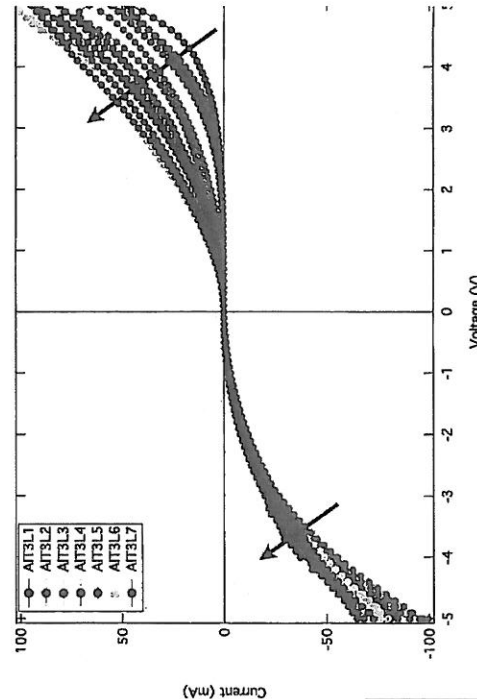
Mobile Dopant Displacement



Memristor cross-section.

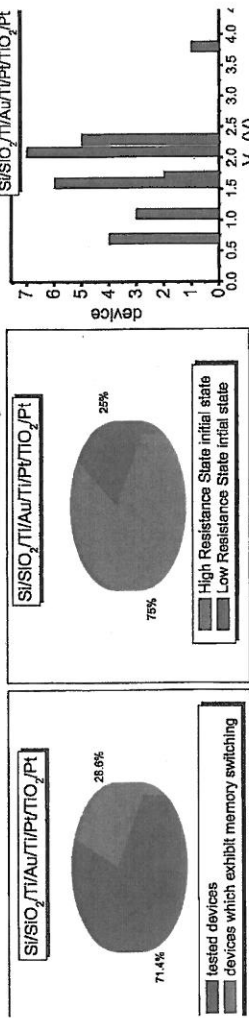


Consecutive Programming

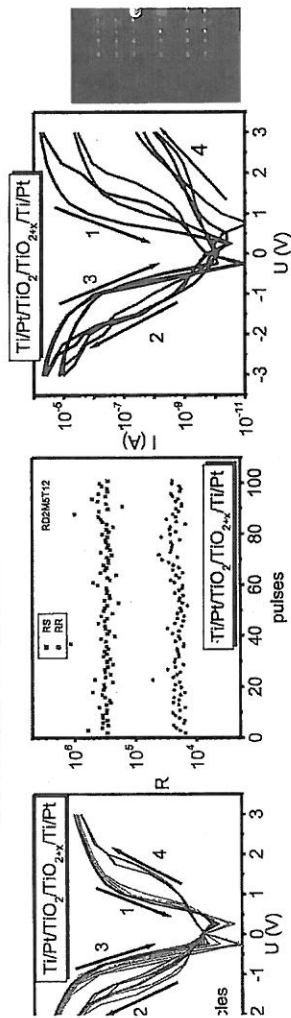


T. Prodromakis et al., unpublished material.

Statistical Analysis



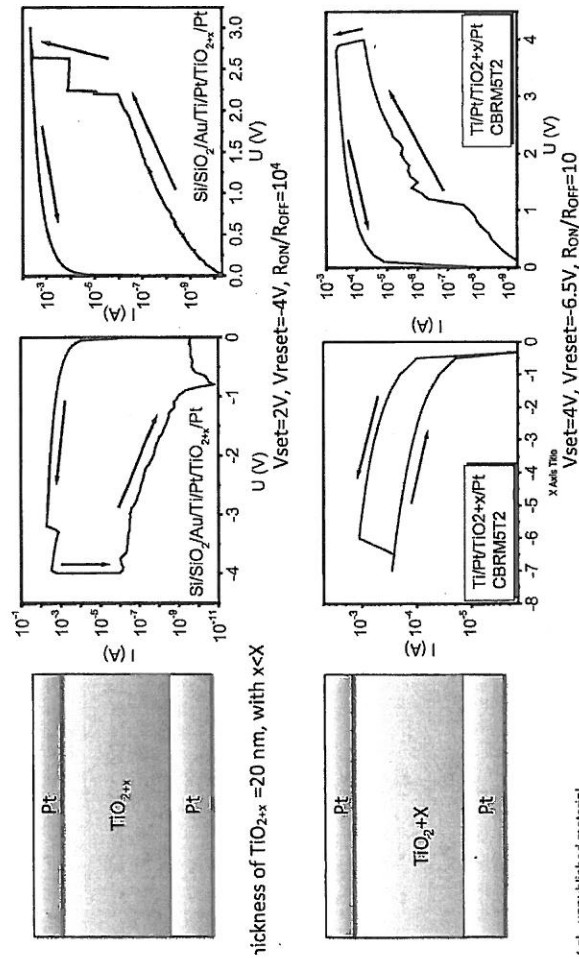
Embedding the bottom electrode within the oxide layer



t al., unpublished material.

Switching thresholds: bipolar switching

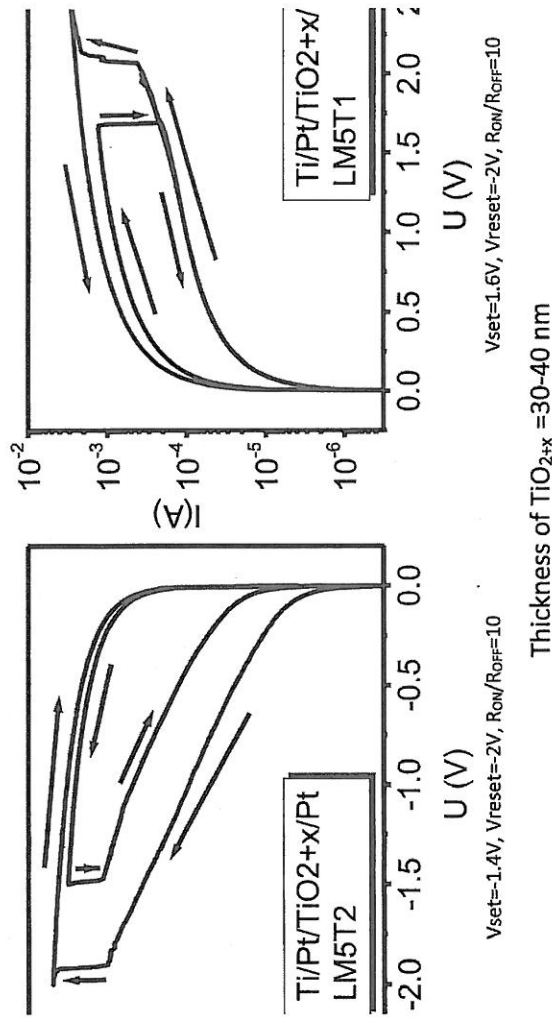
TiO_2 memristors with O_2 excess



t al., unpublished material.

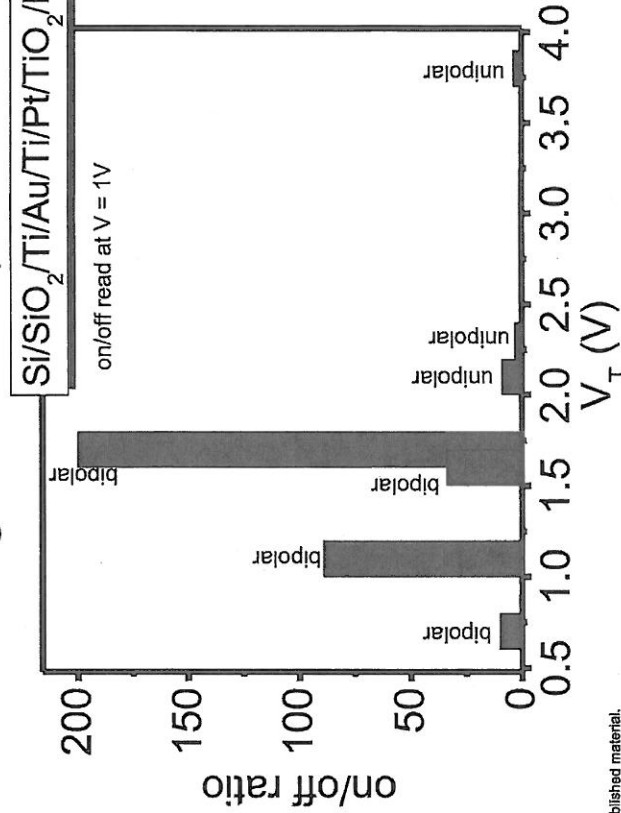
Switching thresholds: unipolar switching

TiO_2 memristors with O_2 excess



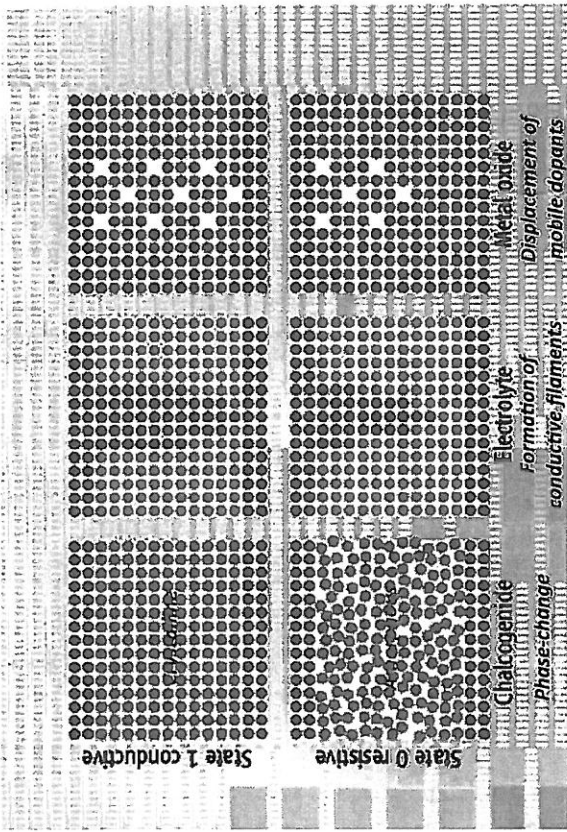
t al., unpublished material.

Switching thresholds dependencies



t al., unpublished material.

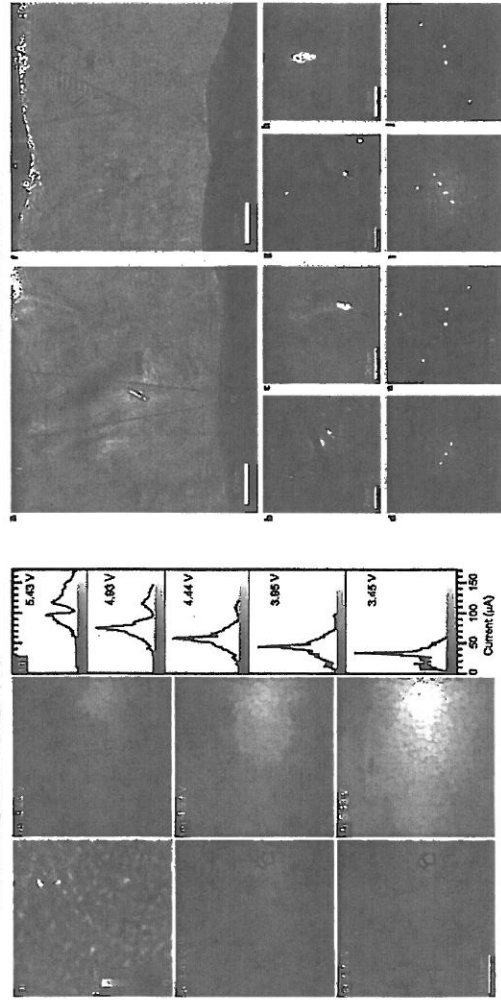
Switching mechanisms of distinct systems



as the Nonvolatile Memory Race", Science, vol. 319 pp. 1625-6, 2008.
in, G. Selkov and K. Sato, "Redox-Based Resistive Memories - Nanionic Mechanisms, Prospects, and Challenges", Adv. Mater., vol. 21, pp. 2652-2663, 2009.

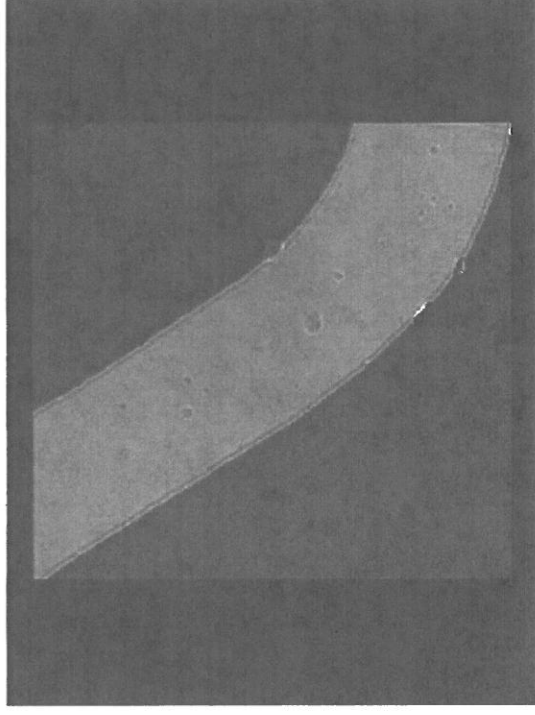
Switching validation

Conducting AFM topography



Physics Letter 96, p. 213106, 2010
Atomic structure of conducting nanofilaments in TiO₂ resistive switching memory", Nat. Nanotechnology, vol. 5, no. 2, pp. 148-153, 2010.
mechanism of electroforming of metal oxide memristive switches", Nanotechnology, vol. 20, 215201, 2009.

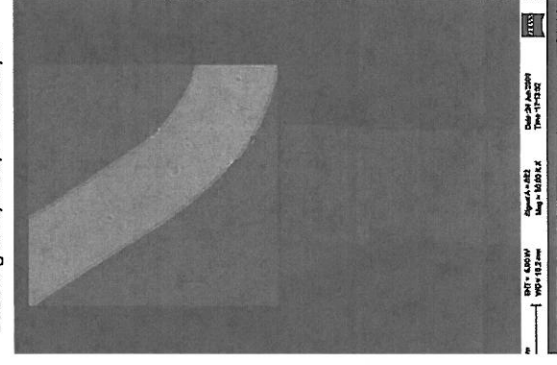
Switching validation



Physics Letter 96, p. 213106, 2010
Atomic structure of conducting nanofilaments in TiO₂ resistive switching memory", Nat. Nanotechnology, vol. 5, no. 2, pp. 148-153, 2010.
mechanism of electroforming of metal oxide memristive switches", Nanotechnology, vol. 20, 215201, 2009.

Switching validation

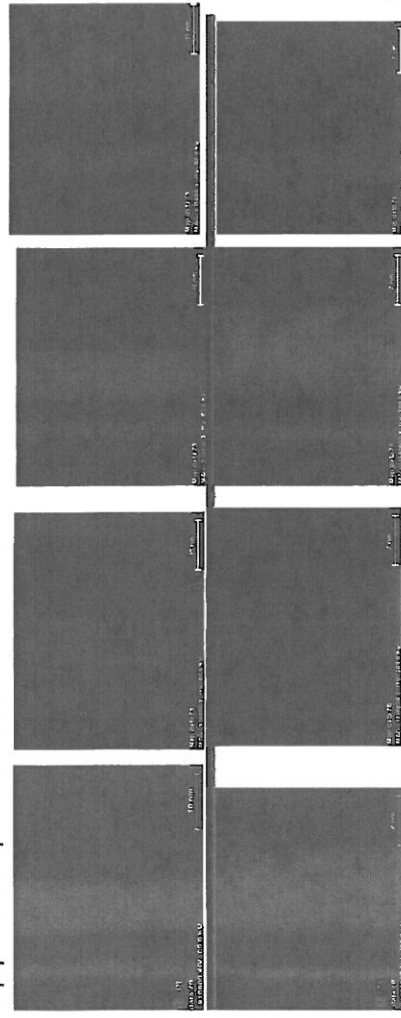
Bubbling in Pt/TiO₂/Pt multilayer



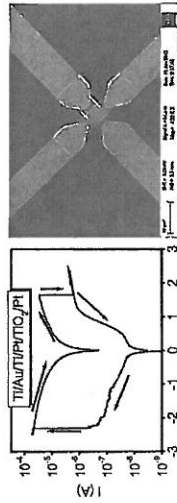
High-resolution TEM

Physics Letter 96, p. 213106, 2010
Atomic structure of conducting nanofilaments in TiO₂ resistive switching memory", Nat. Nanotechnology, vol. 5, no. 2, pp. 148-153, 2010.
mechanism of electroforming of metal oxide memristive switches", Nanotechnology, vol. 20, 215201, 2009.
at... unpublished material.

Top pictures - pristine device



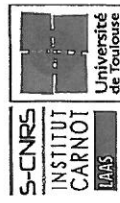
30bottom pictures Tested device



4) unsubstantiated material

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for Bio-Inspired Technology

Institute of
Organic Chemistry

- D1.1** (9m) Fabrication of single memristor cells
D1.2 (12m) Memristor model with detailed specifications (R_{ON}/R_{OFF} , V_T)
D1.3 (24m) Fabrication of 2-D memristive grids
D1.4 (36m) Process flowchart and preliminary monolithic specimens

- D2.1** (6m) Neuron specifications
D2.2 (12m) Neuron design sent for fabrication
D2.3 (24m) Neuron array sent for fabrication
D2.4 (36m) Test of hybrid CMOS-memristive system

- D3.1 (6m) Specifications for synaptic CMOS and memristive circuits
D3.2 (12m) Hybrid CMOS/memristive neuromorphic synapse circuits
D3.3 (24m) Hybrid CMOS/memristive spike-based learning device
D3.4 (36m) Spike-based learning system characteristics and demo

- D4.1 (24m)** Report on novel brain-inspired paradigms for computation and self-organization in neuromorphic systems.
D4.2 (36m) Report on possible applications of self-adapting circuits.

- D5.1 (6m) Interfacing of prototypes/Fabrication of NIL masks
- D5.2 (16m) First integrated CMOS/memristor platforms (single-elements)
- D5.3 (30m) Integrated CMOS/Memristor platforms (networks)
- D5.4 (36m) Monolithic integration approach

Work-Packages		Y1				Y2				Y3							
		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4				
1	Fabrication of single-memristors																
	Fabrication of memristive glide																
	Monolithic integration																
	Single-neuron design																
2	Design of neural array																
	Test of hybrid platform																
3	Biophysics of synapses/neurons																
	Modelling of synaptic dynamics																
	Spike-based plasticity circuits																
	Learning mechanisms evaluation																
4	Develop computation paradigms																
	Self-adapting applications																
5	Interfacing of prototypes																
	Integration of CMOS/memristors																
	Monolithic integration on CMOS																
Milestones		M1 M2				M3				M4							

D6.1:3 (12m, 24m and 36m) Progress reports

- M1 Determination of true neural/synapses biophysics.
- M2 Experimental demonstration of STDP via single memristor elements.
- M3 Development of novel computation paradigm.
- M4 Experimental demonstration of cognition.

PNEUMA is the first of its kind within EU

aiming at linking distinct disciplines unconventionally

Memristors are indeed a disruptive technology with great potential but also bare many challenges

it's relatively easy to demonstrate memristive behaviour, but rather difficult to do it in a reliable manner!

PNEUMA aims to mature this technology

within a neurobiological perspective (high-risk but high-payoff)

he strength (interdisciplinarity) of PNEUMA can also be its weakness alleviate this by having targeted interactions within the different groups have also set-up an advisory board to enhance the external visibility PNEUMA but also outsource expertise when & if needed!